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AMENDMENTS TO THE CLAIMS

Please cancel claims 22-32. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Previously Presented) A switching apparatus for sharing input/output endpoints, the switching apparatus comprising:

   a first plurality of I/O ports, coupled to a plurality of operating system domains (OSDs) through a load-store fabric, each configured to route transactions between said plurality of OSDs and the switching apparatus;

   a second I/O port, coupled to a first shared input/output endpoint, wherein said first shared input/output endpoint is configured to request/complete said transactions for each of said plurality of OSDs; and

   core logic, coupled to said first plurality of I/O ports and said second I/O port, configured to route said transactions between said first plurality of I/O ports and said second I/O port, wherein said core logic designates a corresponding one of said plurality of OSDs according to a variant of a protocol, and wherein said variant comprises encapsulating an OS domain header within a transaction layer packet that otherwise comports with said protocol, and wherein said protocol provides for routing of said transactions only for a single OSD.

2. (Cancelled)

3. (Original) The switching apparatus as recited in claim 1, wherein said first plurality of I/O ports communicates with said plurality of OSDs according to said protocol.

4. (Original) The switching apparatus as recited in claim 1, wherein said protocol comprises PCI Express.

5. (Original) The switching apparatus as recited in claim 4, wherein said core logic isolates said transactions over a plurality of PCI Express bus hierarchies according to said each of said plurality of OSDs.

6. (Original) The switching apparatus as recited in claim 5, wherein a subset of said transactions are routed in accordance with addressing mechanisms for a particular one of said plurality of PCI Express bus hierarchies, said particular one of said plurality of PCI Express bus hierarchies corresponding to a particular one of said plurality of OSDs.

7. (Previously Presented) The switching apparatus as recited in claim 1, wherein said core logic is configured to associate each of said transactions with a corresponding one of said plurality of OSDs, said corresponding one of said plurality of OSDs corresponding to one or more root complexes.

8. (Original) The switching apparatus as recited in claim 7, wherein said transaction layer packet is routed between said second I/O port and said first shared input/output endpoint.

9. (Original) The switching apparatus as recited in claim 8, wherein said first shared I/O endpoint is configured to detect said OS domain header and to perform a specified operation according to said protocol exclusively for said one of said plurality of OSDs.

10. (Original) The switching apparatus as recited in claim 1, wherein said first shared input/output endpoint designates one of said transactions for a particular one of said plurality of OSDs by encapsulating an OS domain header within a transaction layer packet, and wherein said transaction layer packet is routed to said core logic via said second I/O port.

11. (Original) The switching apparatus as recited in claim 10, wherein said core logic is configured to detect and decapsulate said OS domain header from said transaction layer packet, and is configured to route said one of said transactions to said particular one of said plurality of OSDs according to said protocol.

12. (Previously Presented) A shared input/output (I/O) switching mechanism, comprising:

core logic, configured to enable operating system domains to share one or more I/O endpoints over a load-store fabric, said core logic comprising:

global routing logic, configured to route first transactions to/from said operating system domains, and for routing second transactions to/from said one or more I/O endpoints, wherein each of said second transactions designates an associated one of said operating system domains for which an operation specified by each of said first transactions be performed, and wherein said associated one of said operating system domains is designated according to a variant of a protocol, and wherein said variant comprises encapsulating an OS domain header within a transaction layer packet that otherwise comports with said protocol, and wherein said protocol provides exclusively for a single operating system domain within said load-store fabric.

13. (Cancelled)

14. (Original) The shared I/O switching mechanism as recited in claim 12, wherein said protocol comprises PCI Express, and wherein said first transactions comport with said protocol.

15. (Original) The shared I/O switching mechanism as recited in claim 14, wherein said core logic isolates said first and second transactions over a plurality of PCI Express bus hierarchies according to each of said operating system domains.

16. (Original) The shared I/O switching mechanism as recited in claim 15, wherein said first and second transactions are routed in accordance with addressing mechanisms for a particular one of said plurality of PCI Express bus hierarchies, said particular one of said plurality of PCI Express bus hierarchies corresponding to said associated one of said operating system domains.

17. (Original) The shared I/O switching mechanism as recited in claim 12, wherein said core logic associates each of said operating system domains with each of a corresponding root complex.

18. (Previously Presented) The shared I/O switching mechanism as recited in claim 12, wherein said transaction layer packet is routed between said the shared I/O switching mechanism and one of said one or more I/O endpoints.

19. (Original) The shared I/O switching mechanism as recited in claim 18, wherein said one of said one or more I/O endpoints is configured to detect said OS domain header and to perform said operation according to said protocol exclusively for said one of said operating system domains.

20. (Original) The shared I/O switching mechanism as recited in claim 12, wherein one of said one or more I/O endpoints designates one of said second transactions for a particular one of said operating system domains by encapsulating an OS domain header within a transaction layer packet, and wherein said transaction layer packet is routed to the shared I/O switching mechanism.

21. (Original) The shared I/O switching mechanism as recited in claim 20, wherein VMAC logic within the shared I/O switching mechanism is configured to detect and decapsulate said OS domain header from said transaction layer packet, and wherein said core logic routes a corresponding one of said first transactions to said particular one of said plurality of operating system domains according to said protocol.

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)